Yihua Liu

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EDUCATION

Shanghai Jiao Tong University (SJTU), Shanghai, China

Sept. 2018 – Aug. 2022

Bachelor of Science, Electrical and Computer Engineering, Cumulative GPA: 3.23/4.0

Undergraduate Research: A, Data Science: A, Microprocessor Design: A-, Linear Algebra: A-, Computer Vision: A-, Computer Architecture: A-, Advanced Embedded System: A-

Shanghai Jiao Tong University (SJTU), Shanghai, China

Sept. 2022 – Present

Bachelor of Master, Electronic Science and Technology, Cumulative GPA: 3.85/4.0

- Introduction to Engineering Numerical Analysis: A
- TA of ECE4810J System-on-Chip Design: Design and complete 3 FPGA labs, 3 ASIC labs, and 1 project, covering Vitis HLS, Vitis, PYNO, MATLAB HDL Coder/Simulink, PyMTL, OpenROAD, OpenLane, Synopsys, etc.

RESEARCH EXPERIENCES

Design of Integrated Micro-robotic Fish, VE490 Undergraduate Research (Prof. Xuyang Lu) Feb. 2021 – Apr. 2021 Design and fabricate a microfluidic chip and channel

Simulate and verify the performance of the chip by MATLAB and COMSOL Multiphysics

Optimization of Placement and Routing in VLSI, Research Intern (Prof. Xinfei Guo)

May 2021 - Dec. 2021

Pull request to DREAMPlace, deep learning toolkit-enabled VLSI placement

SELECTED PROJECTS

MIPS Processor Design, VE370 Intro to Computer Organization

Nov. 2020

- Project 2: Implement a five-stage pipeline with forwarding unit and hazard detection unit (Verilog & FPGA Demo)
- Project 3: Design caches both direct-mapped and 2-way-associative with write-through or write-back (Verilog)

VS Code Sidebar Multilingual Smart Reader Extension (vscode-covert-reader)

Dec. 2020 - Jan. 2021

Gesture-Controlled Mantis Robot, VE373 Design of Microprocessor Based Systems

July 2021

Final Project: Build a gesture-controlled robot that can avoid obstacles using PIC32 MCU and Arduino

Operating System Projects, VE482 Introduction to Operating Systems

Sept. 2021 – Dec. 2021

- Project 1: mumsh shell, support redirection, pipes, quotes parsing, signals, background, error handling, etc.
- Project 2: lemondb multithreaded database
- Project 3: Minix 3.2.1 kernel lottery and EDF scheduling with keys and kernel params switching

Early-Exit Offloading for Embedded Question Answering Applications, ECE4730J Advanced Embedded System Capstone Design, leader & main contributor, repo: vihuajack/ECE4730J FA2021 (github.com) Oct. 2021 - Dec. 2021 Entropy-based early-exit for PyTorch ALBERT model evaluated by SQuAD 2.0 on Jetson TX2 and VMware Bitfusion Intel P6-Style Out-of-Order RISC-V Processor Design, ECE4700J Computer Architecture Oct. 2021 - Dec. 2021

Final Project: Implement the RV32IM ISA by SystemVerilog, verified by Vivado, including ROB and LSQ

HONORS & AWARDS

Best Technology Award of Project Design in the 2019 Summer Vg100	August 2019
2019-2020 The Excellent League Member of Shanghai Jiao Tong University	May 2020
Student Development Scholarship of SJTU Joint Institute for 2019-2020 academic year	June 2020
UM-SJTU Joint Institute 2020-2021 Undergraduate Excellent Scholarship	November 2021
UM-SJTU Joint Institute 2022 Master's Academic Scholarship	November 2022

SKILLS & CERTIFICATION

English: TOEFL 97 (Reading: 30/Listening: 25/Speaking: 17/Writing: 25)

Languages: skilled in C/C++, GTK/GLib/GObject, LaTeX, MATLAB, Python, SystemVerilog;

familiar with Bash, HTML/CSS, Mathematica, SQL, JavaScript/TypeScript;

basic knowledge of GNU Make/CMake, Lisp/Scheme, PostScript, Tcl, etc.

Software: Capture CIS, COMSOL Multiphysics, KLayout, Multisim, Vitis, Vitis HLS, Vivado, Visio, etc.

Skills: Git, Linux, simple driver development, any editor/IDE (JetBrains, Vim, etc), usually using Windows/WSL/Ubuntu Coursera: Python for Everybody, Machine Learning, Deep Learning, Deep Learning, Deep Learning AI TensorFlow Developer, GANs

Others: Opensource Contributions, Cppreference contributor, experiences in COMAP's Mathematical Contest in

Modeling (MCM2019, MCM2020, MCM2021)